REMARKS

Withdrawal of the finality of rejection, reconsideration and allowance of outstanding claims 1-22 in view of the following remarks are requested.

A. Rejections of Claims 1-22 under 35 USC §102(e)

The Examiner has rejected claims 1-22 under 35 USC §102(e) as being anticipated by U.S. Patent Application Publication Number US 2002/0042909 A1 to Van Gageldonk, et al. ("Van Gageldonk"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by independent claims 1, 7, 11, and 19, is patentably distinguishable over Van Gageldonk.

As disclosed in the present application, conventional approaches in the processor architecture field do not adequately address the problem of consumption of chip area for wide buses, such as wide "move" buses linking various register file banks. Various embodiments according to the present invention address and overcome the need in the art for speeding up the very long instruction word ("VLIW") processor architecture, reducing power consumption, and reducing chip area while accommodating multiple register file banks and multiple execution units.

Embodiments according to the present invention, as shown in Figure 2 of the present application, include first and second register file banks. The first register file bank comprises a first plurality of read ports, and the second register file bank comprises a second plurality of read ports. A first data path block comprises a first plurality of

execution units, and a second data path block comprises a second plurality of execution units. A first plurality of buses couple the first plurality of read ports to each of the first and second data path blocks. A second plurality of buses couple the second plurality of read ports to each of the first and second data path blocks. An operand residing in the first plurality of read ports is concurrently accessed by the first plurality of execution units in the first data path block and by the second plurality of execution units in the second data path block.

In a conventional VLIW processor there are "move" buses that carry source operands from one register file bank to the other. This architecture consumes one or more additional clock cycles and accordingly reduces the operating speed of the conventional VLIW processor. Additionally, transfer of a source operand in this manner results in significant additional power consumption in the conventional VLIW processor since a "toggling" of potentially all of the bits (e.g. 64 bits) in a move bus might occur in order to complete the transfer of the source operand between register file banks. See, for example, present application at page 11, and Figure 1.

There are advantageously no move buses in the VLIW processor according to embodiments of the present invention, as explicitly set forth in the present application. See, for example, present application at page 14. In the present embodiments, due to the fact that operands are delivered directly from either register file bank to either data path block, the additional clock cycle required to move an operand from one register file bank to the other register file bank prior to the delivery of the operand to the destination data

path block is eliminated. Since operands do not go through move buses 170 and 172 (Figure 1 of the present application), increased speed is achieved due to the elimination of the additional clock cycle existing in a conventional VLIW processor. Moreover, the charging and discharging of these buses for the purpose of accomplishing a move is avoided, and as such, a substantial power savings is achieved. Thus, by replacing move buses 170 and 172 (Figure 1 of the present application) in a conventional VLIW processor with read buses 260, 262, 264, and 266 in VLIW processor 200 (Figure 2 of the present application), embodiments of the invention achieve increased speed and reduced power without increasing the required chip area.

In contrast, Van Gageldonk is directed to a retargetable compiling system and method. As seen in Figure 1, Van Gageldonk discloses a first functional unit cluster UC1 and a second functional unit cluster UC2 that share a first register file RF1, where RF1 contains a number of physical registers. See, for example, Van Gageldonk, paragraph 25, paragraph lines 1-9. Van Gageldonk also discloses possible organizations of these physical registers within RF1, but fails in all respects to disclose the novel area and power efficient busing architecture between its functional unit clusters and its register files as disclosed in the present application and as achieved by the VLIW processor architecture claimed by independent claims 1, 7, 11, and 19 of the present application. See, for example, Van Gageldonk, paragraph 25, paragraph lines 9-25.

For example, as seen in Figure 2 of the present application, data path blocks 212 and 214 are configured such that they are only able to write data to an adjacent register

file bank. In this case, data path block 212 can only write to register file bank 252, while data path block 214 can only write to register file bank 254. Since the busing architecture claimed in the present application allows other data path blocks, for example data path block 214 in Figure 2, to read particular data written to a "remote" register file bank 252 via read buses 264 and 266, a considerable area savings results as, focusing on Figure 1, the 32-bit wide write buses 162 and 164 that are found in conventional VLIW processors can be eliminated. See, for example, the present application, page 16, lines 11-16. In addition, this configuration adds flexibility as to where the results of operations performed in a particular data path block can be written. For example, data is equally available to both data path blocks 212 and 214 whether data is written into, and hence read from, register file bank 252 or 254. As such, there is no need to ensure that the result of an operation is written to a register file bank where the data is most likely to be read from. See, for example, the present application, page 16, lines 3-11.

Van Gageldonk, however, merely teaches a general configuration where two functional unit clusters UC1 and UC2 access a register file RF1 containing a "visible" sub-register file RF1', without teaching the power and area efficient busing architecture between its functional unit clusters and its register files as defined by independent claims 1, 7, 11, 19. For example, Van Gageldonk does not disclose or suggest an ability of functional unit cluster UC1 to read data from either register file RF1 or RF1'. As show in Figure 1 of Van Gageldonk, UC1 can read data only from the "visible" sub-register file RF1' and not from the invisible register file RF1. However, the present invention

discloses and claims this ability in that, for example, data path block 212 can read data from either adjacent register file bank 252 or remote register file bank 254. Therefore, the present invention is patentably distinguishable over Van Gageldonk.

For the foregoing reasons, Applicants respectfully submit that the present invention as defined by independent claims 1, 7, 11, and 19 is not taught, disclosed, or suggested by the cited art. As such, the claims depending from independent claims 1, 7, 11, and 19 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 7, 11, and 19, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to all claims 1-22 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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